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12. (Amended) The method according to claim 10, further including a seventh step for substituting a defective portion with a relieving circuit according to the result of inspection by said fourth step.

13. (Amended) The method according to claim 10, wherein after the protruding electrodes are formed in said second step and the testing pads are formed in said third step, the burn-in in said fifth step is effected on pieces diced in said sixth step.

14. (Amended) The method according to claim 10, wherein after the testing pads are formed in said third step, the burn-in is executed in said fifth step, the protruding electrodes are formed in said second step and the dicing is performed in said sixth step.

REMARKS

Examination is requested.

Respectfully submitted,

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**MARKED UP VERSION OF REWRITTEN CLAIMS**

3. (Amended) The semiconductor integrated circuit device according to claim 1 [or 2], wherein said conductive layers are metal wirings, said insulating film is formed on said each metal wiring, and an insulating film is further formed below said each metal wiring.

7. (Amended) The semiconductor integrated circuit device according to claim 1 [or 2], wherein said testing pads are placed just above said terminals corresponding thereto.

9. (Amended) The semiconductor integrated circuit device according to claim 1 [or 2], wherein said testing pads extend on said insulating film.

12. (Amended) The method according to claim 10 [or 11], further including a seventh step for substituting a defective portion with a relieving circuit according to the result of inspection by said fourth step.

14. (Amended) The method according to claim 10 [or 11], wherein after the testing pads are formed in said third step, the burn-in is executed in said fifth step, the protruding electrodes are formed in said second step and the dicing is performed in said sixth step.